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A Review: Performance analysis and design of wideband CMOS voltage controlled ring oscillator

Rajkumar Tiwari[1] Mishra Jyoti[2]
[1]*Prof. Department of physics Dr RMLU Avadh University Faizabad*
[2]*Research scholar Dr RMLU Avadh University Faizabad*

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ABSTRACT:- Voltage controlled ring oscillators using differential topology are designed and implemented for distinct applications using CMOS technology with the several characteristics. But all have distinct behaviours like some merits and demerits and correlate to every other. This paper defines a performance analysis of voltage controlled ring oscillators (VCRO) supported many differential delay systems in term of broad tuning range and low power consumption at below 1V input supply. This relative analysis shows the simulative results of four kinds of VCROs. within which one of them has low power consumption i.e. minimum 0.34uW for low power applications and rest has maximum tuning range 1.22 GHz to 3.22 GHz for broadband applications using CMOS technology as compare to others.

Keywords- Ring oscillator, Differential delay system, Wide tuning range, Low power consumption , voltage controlled oscillator , inverter, Phase locked loop , Delay locked loop.

I. INTRODUCTION:-

From the sooner decennium of year, the VCOs are very approved building blocks in modern electronics industries for broadband communication uses and biomedical uses. The VCOs are generally construct to style distinct systems like Clock Recovery Systems, Phase Locked Loop Systems, and Frequency Synthesizers systems etc. The voltage controlled oscillator requires double operating frequency to attain 50% duty cycle at high speed. Which makes strenuous the designing of low power PLL systems . Hence it's very demanding and difficult task to style ultra low power consumption with high tuning range VCOs for low power broadband uses. nowadays, VCOs are designed and performed with the assistance of inconsistent topology like- Differential topology, Current starved (CS) topology, Single ended topology, RC and LC topology, Body bias and Replica bias topology etc. for particular applications. This paper shows the relative analysis of outlined five VCROs on the idea of differential topology with several number of delay stages. The simulated result evaluated in term of wide tuning range and low power consumption. The merit of 5 distinct VCRO are discussed in section 2. All needed structures along with simulated results are differentiated and evaluated in section 3 with the conclusion in section 4.

Delay cells for voltage controlled differential ring oscillator:- VCO has a delay cell joined by single ended topology and differential topology. within the single ended ring topology shown in fig-1, during which the odd number of delay cell is joined within the interpretation form just like the output of last stage is that the input of first stage. The best condition for the sustained oscillations must be fulfilled which suggests 360° total phase shift round the loop and unity loop profit which is explained by the Barkhausen principle.

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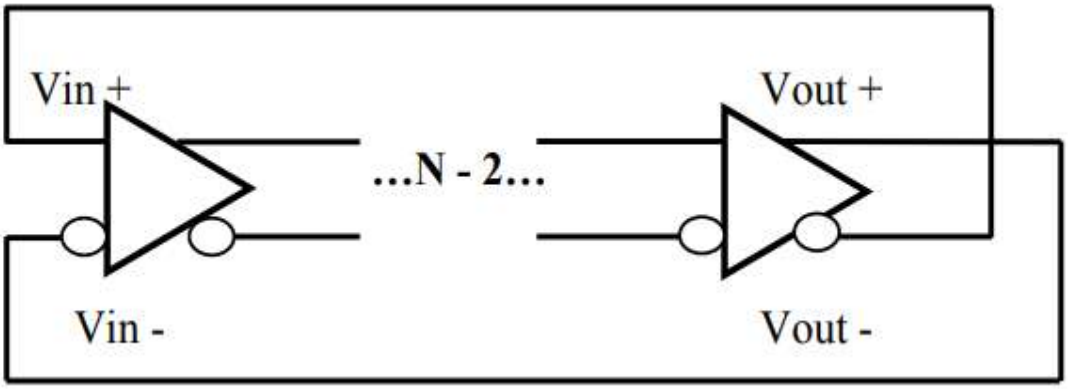

Fig.1 N-stages differential ring oscillator [20]

According to the differential ring topology shown in fig-2, supplied different phases (45◦ , 90◦ , 180◦….). The phase difference between input and output voltage is needed 225◦ for oscillation condition

Hence, oscillations frequency of N stages is:
fo = 1/2Ntd
Where, N = total number of delay cell
td =delay time of every delay cell

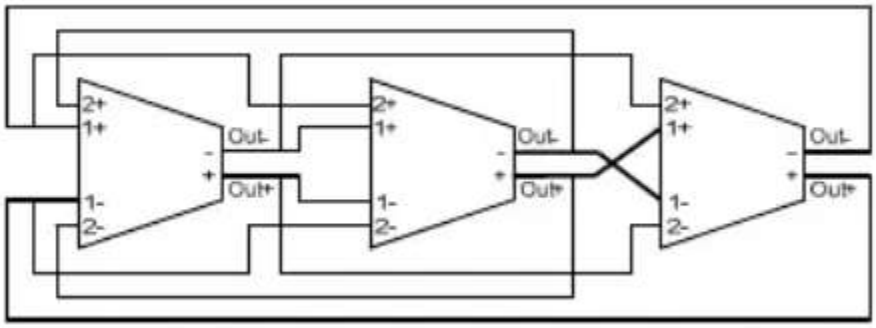

Fig. 2 Block diagram of the proposed differential ring oscillator with feed-forward technique [22]

The differential ring topology for VCO is applicable to reject the common mode noise and ignored bypass coupling capacitors good stability and high frequency. Differential ring oscillator is formed of a load, which has both active and passive elements . It's on great demand for wide tuning range, constant voltage swing, and low power consumption with very low noise. The differential delay system shown in fig. 2 is employed to outlined VCO with three stage delay cell.

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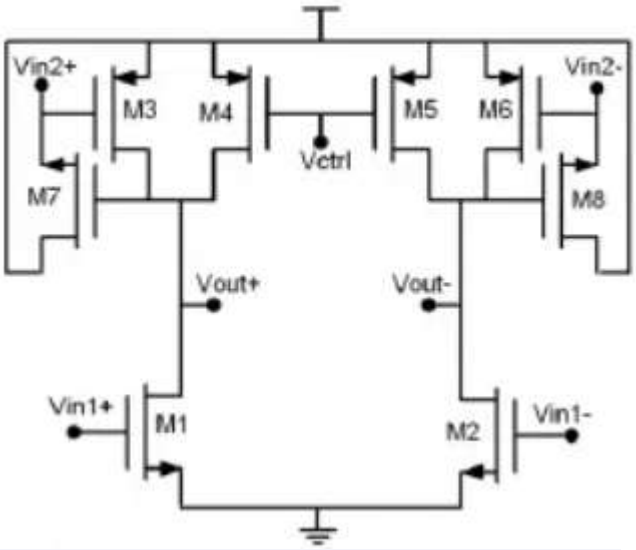

Fig.3 Differential Delay cell used in proposed ring oscillator [23]

The NMOS transistors M7 and M8 are applicable as a load behind M3 and M6 to create a composite load [22], indicating inductive impedance at the drain of M3 and M6. This delay system is made public with two PMOS transistors utilize from deep triode region to saturation region and adjusted with Vgs of transistor. While two NMOS transistor is worked in mere saturation region. The outlined VCRO using this differential delay cell is incredibly mendatory to extend tuning range and minimize the power consumption .By using this delay system, 3 stage VCRO has been designed for the broad tuning range 0.80GHz-11.64GHz with low power consumption 68.60µW at 1.2V input supply and 4.32 µW at 0.8V in 2014 [6]. While someone has designed the 5 stage, 7 stage, 9 stage differentials VCRO by using simple CMOS delay cell shown in fig-4.

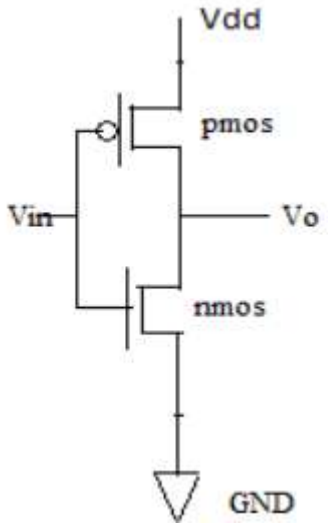

fig-4 CMOS delay cell for differential vcro [8]

CMOS delay cell is created of complementary MOS transistors. Where PMOS works as a load and NMOS works as driver for prime current gain. These PMOS and NMOS behaves similar like channel length, doping. This delay cell works as a Inverter means Vin = 0 then Vo =1 and vice-versa [8]. The differential VCRO using simple delay cell gives high frequency range up to MHz with power consumption in µW (min 0.34 µW). But this tuning range is tiny as compare to other for wide application. In year 2016, the low phase noise has been designed by B.S. Patro, wide

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tuning range differential VCRO for signal processing. He has designed suggested delay cell for particularly high signal processing system shown in fig-5.

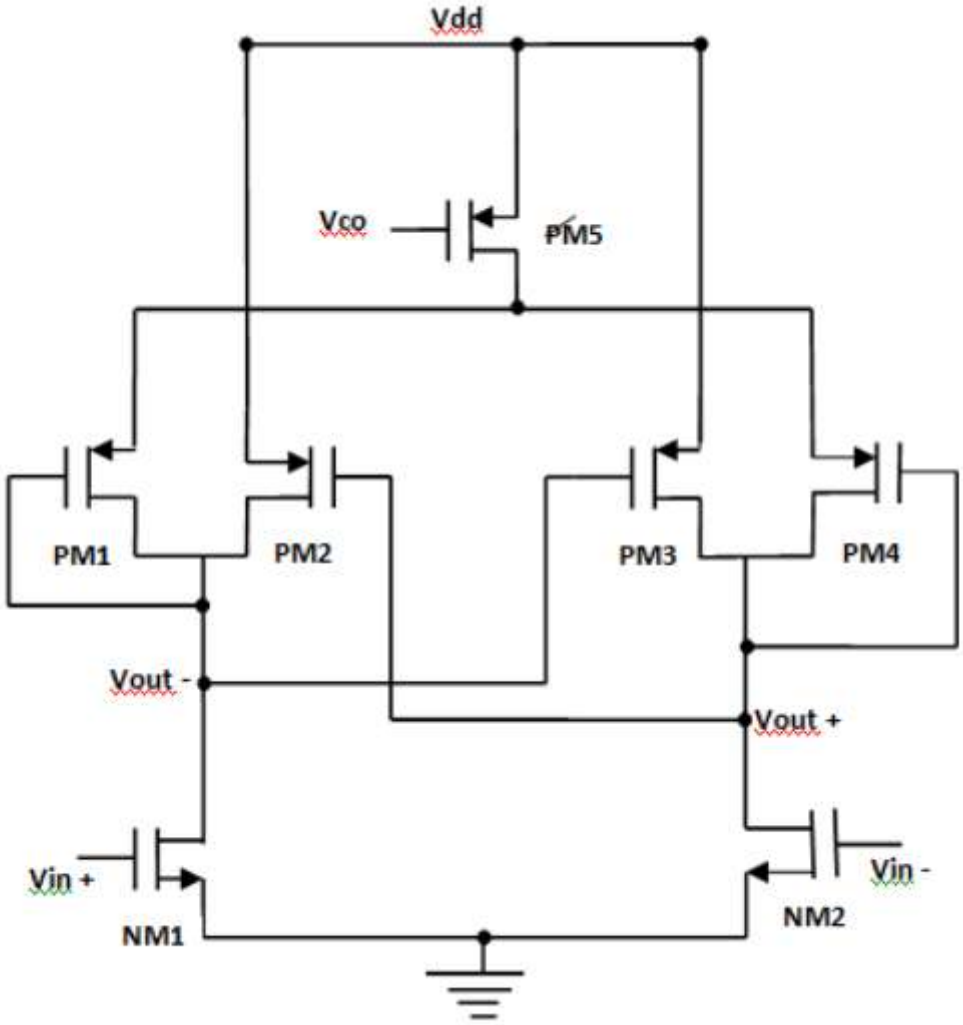

Figure 5.Schematic of delay cell offered [21]

The differential pair of P2 and P3 is applicable in regeneration feedback format to decrease the delay and increase the speed in oscillation of oscillator. The oscillator frequency may controlled by the Vc given in P0 and P1. The negative feedback circuit rather than positive feedback can induce much stability with high speed but absorb more power. Therefore, this configuration of delay cell with positive feedback is helpful to ignore the appliance of current mirror. The differential VCRO using this delay cell gives the wide tuning range of 2.5GHz-7.7GHz and low power consumption 2.18 µW with very low phase noise of -96.47dBc/Hz [21]. currently in 2019, Esteban Tlelo - Cuautle has outlined the wide band VCRO with current-mode logic gate supported differential topology. It is executed on CMOS technology. This current mode logic gate as a delay cell is meant in fig-6.

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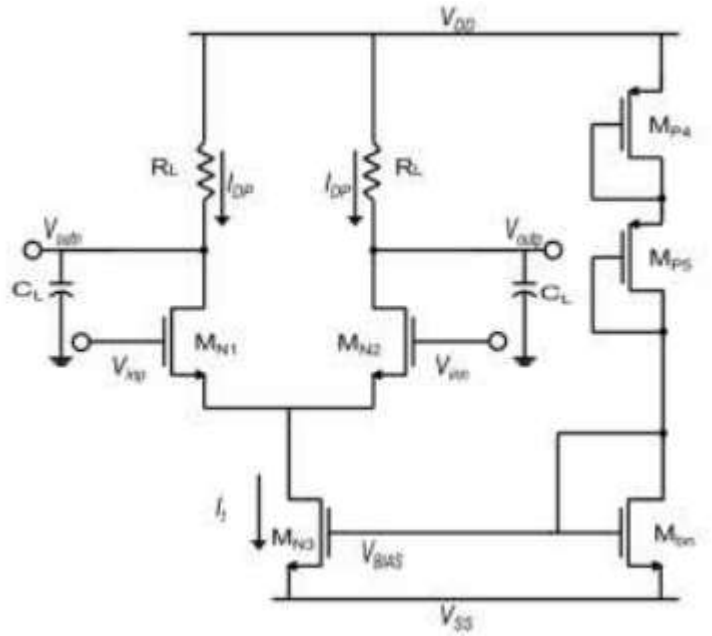

fig-6 common mode logic gate as a delay cell for differential vcro [11]

The oscillation frequency of this VCRO is oppositely relied on the number of common mode logic gate N and therefore the propagation delay time td. The delay will be decreased by transconductance of transistor with low equivalent capacitance. This VCRO gives the frequency ranges of 2.65–5.65 GHz with low power consumption [11].

Result of Simulation:- The four sorts of differential voltage controlled ring oscillator outlined using distinct delay cell for wide band uses and simulated on different technology. The voltage controlled ring oscillator using delay cell shown in fig-3 is simulated in LT spice tool. The highest power dissipation is 68.66 µW at 1.2 V input provide and minimum dissipation is 4.40 µW at 0.8 V input provides with 0.5V control voltage While differential voltage controlled ring oscillator using simple CMOS delay cell shown in fig-4 is simulated on cadence virtuso tool. For a voltage controlled ring oscillator, propagation delay may be a necessary factor.

fig- 7 power consumption analysis by bar graph[7]

The power consumption evaluation by the Bar chart is shown in above fig- 7 which shows that it have minimum consumption of power (0.34uW) for the 5-stage differential VCRO using Simple CMOS delay cell. When the stages of delay cell is increased then power consumption will increase at the identical time. it gives calculated phase noise -96.148 dBc/Hz at 1 MHz offset. It's

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very small when tuned correctly. The differential Voltage controlled ring oscillator by using Common mode gates(shown in fig-6) gives the oscillations between 2.65 GHz and 5.65 GHz by changing control voltage 0.2 V -0.9 V. which could be a broad tuning range with 39mW power consumption.

Table 1: Performance analysis table

Ref. and year	Process technology	Stages	Tuning range	Power consumption
[7] 2014	50nm CMOS Technology	3	0.80GHz - 11.64GHz	4.32µW at 0.8V
[8] 2016	45nm CMOS Technology	5 7 9	1032MHz 831MHz 751MHz	0.34 µW, 0.48 µW, 0.61 µW
[10] 2016	45nm CMOS Technology	2	2.5 GHz-7.7 GHz	2.18uW
[11] 2019	180nm CMOS Technology	4	2.65 GHz-5.65 GHz	39mW
[17] 2020	65nm CMOS Technology	3	10.14GHz – 28.5GHz	0.02 mW
[5] 2021	28nm CMOS Technology	3 5 7	1MHz -1GHz 516MHz 360 – 640MHz	29 µW.

II. CONCLUSION:-

Many kinds of differential VCROs has been outlined by the authors supported several delay system. But mostly utilized differential VCRO is discussed here during this review paper. From which, differential delay system utilized in [7] and [8] are very efficient and reliable for the broad tuning range (maximum 11.64GHz) and low power consumption (minimum 0.34uW) consequently in broadband signal processing uses as compare to others VCOs yet.

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